UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,737	03/24/2004	Joe W. Zhao	X-1437 US	5860

24309 7590 06/10/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/808,737	ZHAO ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/808737 filed on 03/24/04.

Claims 1-25 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Calderone et al. (US Patent 6507942).

3. As to claims 1, 21, and 25 Calderone et al. teach a method for monitoring and improving a fabrication process for integrated circuits comprising: instantiating a test pattern on a plurality of configurable devices fabricated on a wafer using the fabrication process (see fig 5 element 505 col 4 lines 1-10); identifying at least one underperforming region in at least one of the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32); determining if the at least one underperforming region is layout sensitive (see fig 5 col 4 lines 1-32); and responsive to the step of determining, adjusting at least one of layout of the at least one of the plurality of configurable devices and the fabrication process (see fig 5 element 535 col 4 lines 1-32 especially line 18-23).

4. As to claim 2 Calderone et al. teach further comprising: dividing each of the plurality of configurable devices into a plurality of regions (see fig 2-5 col 4 lines 1-10).

5. As to claim 3 Calderone et al. teach wherein the step of instantiating a test pattern comprises instantiating a same test pattern in each of the plurality of regions (see fig 5 col 4 lines 1-32).

6. As to claim 4 Calderone et al. teach wherein the step of determining comprises correlating performance of each of the plurality of regions with layout of the each of the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and background).

7. As to claim 5 Calderone et al. teach wherein: if there is a high correlation, adjusting the layout of the at least one of the plurality of configurable devices; and if there is a low correlation, adjusting the fabrication process (see fig 5 element 515 col 4 lines 7-15).

8. As to claim 6 Calderone et al. teach wherein: the step of determining comprises correlating performance of each of the plurality of regions with the wafe r(see fig 5 element 515 col 4 lines 7-15); if there is a low correlation, adjusting the layout of the at least one of the plurality of configurable devices; and if there is a high correlation, adjusting the fabrication process (see fig 5 element 535 col 4 lines 1-32 especially line 7-23).

9. As to claim 7 Calderone et al. teach wherein the test pattern comprises a ring oscillator (see fig 5).

10. As to claim 8 Calderone et al. teach wherein the step of identifying comprises measuring a frequency of the ring oscillator (see fig 5 col 4 lines 1-32).

11. As to claim 9 Calderone et al. teach wherein the step identifying comprises measuring at least one of frequency, delay, voltage, current, and signal quality of each of the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and background).

12. As to claim 10 Calderone et al. teach further comprising: tailoring test pattern to measure performance of interconnections within the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and background).

13. As to claim 11 Calderone et al. teach wherein tailoring the test pattern comprises tailoring the test pattern to measure performance of a particular layer within the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

14. As to claim 12 Calderone et al. teach wherein the copper metal lines. interconnections are copper metal lines (see fig 5 col 4 lines 1-32).

15. As to claim 13 Calderone et al. teach further comprising: tailoring the test pattern to measure performance of transistors within the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

16. As to claim 14 Calderone et al. teach further comprising: applying test vectors to each of the plurality of configurable devices (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary); and analyzing results based on the step of applying test vectors (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

17. As to claim 15 Calderone et al. teach wherein adjusting the layout of the at least one of the plurality of configurable devices comprises adding dummy metal (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

18. As to claim 16 Calderone et al. teach further comprising: after the step of adjusting, repeating the steps of instantiating, identifying and determining (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

19. As to claim 17 Calderone et al. teach wherein the test pattern is also used during the normal testing of the plurality of configurable devices (see fig 5 col 4 lines 1-32).

20. As to claims 18 and 23 Calderone et al. teach wherein the plurality of devices comprises a programmable logic device (see fig 2-5 col 2 lines 61 to col 4 lines 32).

21. As to claim 19 and 24 Calderone et al. teach wherein the programmable logic device is a field programmable logic array (see fig 2-5 col 2 lines 61 to col 4 lines 32).

22. As to claim 20 Calderone et al. teach further comprising: after the step of adjusting, fabricating an integrated circuit different from the plurality configurable devices using the fabrication process (see fig 5 col 4 lines 1-32 and background).

23. As to claim 22 Calderone et al. teach further comprising: a probe card coupled between the tester and the wafer for interfacing between the tester and the wafer (see fig 2-5 col 2 lines 61 to col 4 lines 32 and summary).

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art Unit 2825
June 6, 2005

THUAN DO
Primary examiner
06/07/2005